

Applicant : Yoshinori Hino et al.
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Filed : February 21, 2002
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Attorney's Docket No.: 10417-120001 / F51-
143214M/TOM

REMARKS

Claims 1-7, 10-17 and 18-20 are pending. Claims 1-7 and 10-17 have been amended to clarify the subject matter. Claims 8 and 9 have been canceled. Claims 18-20 have been added. No new matter has been added.

In view of the above amendments and the remarks below, applicants respectfully request withdrawal of the rejections and allowance of the application.

Drawings

The drawings including Figs. 16, 17A, 17B, 17C and 17D have been objected to.

Replacement drawings including Figs. 16, 17A, 17B, 17C and 17D have been submitted. Figs. 16, 17A, 17B, 17C and 17D have been corrected by adding the legend --Prior Art--.

In light of the above corrections, applicants respectfully request withdrawal of the objections.

Specification

The abstract has been objected to.

The abstract has been corrected as suggested by the office action.

In light of the above corrections, applicants respectfully request withdrawal of the objections.

Claim Objections

Claim 1-17 have been objected to for various informalities.

Applicants have amended claims 1-7 and 10-17 as suggested by the office action. Claims 8 and 9 have been canceled.

In light of the above amendments, applicants respectfully request withdrawal of the objections.

Claim Rejections 35 USC 102

Claims 1-3 and 8-13 have been rejected as being anticipated by Bright et al.

Claim 1 has been amended to incorporate features of claim 4. Amended claim 1 recites:

1. (Currently Amended) A pattern layout method of a semiconductor made in one chip with an anode driver, a cathode driver, and memory portions comprising:

laying out drivers connected to the memory portions equally in the chip, **said drivers include a plurality of output regions; and**

arranging each memory portion equally in a vicinity of each of the drivers. (Emphasis Added)

Applicants submit that the above bolded feature is not taught or suggested by the Bright reference for the following reasons. Fig. 1 of the Bright reference shows IO drivers coupled to memory portions 12. However, the drivers do not include “a plurality of output regions” as recited in amended claim 1. Thus, claim 1 is not anticipated by the Bright reference for at least this reason.

Claims 2 and 3 depend on claim 1 and should be allowable for at least the same reasons as claim 1. Claims 4 and 7 are allowable as indicated by the Examiner. Rejections directed to claims 8 and 9 are moot because claims 8 and 9 have been canceled.

Original independent claim 10 has been substituted with new independent claim 19 as described in detail below. Claims 11 –13 have been amended to refer to new claim 19. Claims 19 and 11-13 should be allowable for the reasons described in detail below. Original claim 10 and claims 14-17 are allowable as indicated by the Examiner.

Allowable Subject Matter

Claims 4-7 and 14-17 have been objected to but would be allowable if rewritten to overcome the objections due to minor informalities.

Applicants thank the Examiner for the allowable subject matter. Applicants have amended claims 1-7 and 10-17 to overcome the informalities pointed out in the office action. However, applicants decline to rewrite these claims in independent form.

New Claims

Claims 18 to 20 have been added. These claims are supported by the specifications, claims, and/or drawings in the application. No new matter has been added.

Claim 18 is a combination of claims 1 and 4 and includes language to clarify the output regions as described in the specification. New claim 18 recites:

18. (New) A pattern layout method for a semiconductor chip comprising:

laying out an anode driver and a cathode driver equally in the semiconductor chip, each of said drivers containing a plurality of output regions constituting an output bit group, and each output region corresponding to one bit;

providing a memory portion for each of the drivers; and

forming a dummy pattern adjacent to the output bit group, said dummy pattern having a shape equivalent to the output region. (Emphasis Added)

Applicants submit that the bolded feature is not disclosed, taught or suggested by the cited prior art. The bolded feature is similar to the feature recited in claim 1. Claim 1 should be allowable for the reasons above. Accordingly, claim 18 should be allowable for at least the same reasons as claim 1

New claim 19 includes the features of claim 10, which is based on a combination of claims 8 and 9. New claim 19 recites:

19. (New) A pattern layout method for a semiconductor chip comprising:

disposing drivers at periphery portions of the semiconductor chip, each driver with a plurality of output regions, which constitutes an output bit group, and said output region corresponding to one bit; and

providing wirings for connecting each output bit group of the devices peripherally disposed to circle around within the chip. (Emphasis Added).

Applicants submit that the bolded feature is not disclosed, taught or suggested by the cited prior art. Bright et al.'s Fig. 1 does not disclose providing a wiring that circles around within the chip as recited in claim 19. Thus, claim 19 is not anticipated by the Bright reference.

New claim 20 is dependent on claim 19. Claim 20 recites that the method further provides "memory portions approximately in the center of the semiconductor chip." Claim 20, which is dependent from claim 19, should be allowable for at least the same reason as claim 19.

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In addition, claim 10 has been substituted with claim 19. Claims 11-13, which depended on original claim 10, have been amended to refer to new claim 19. Amended claim 11-13 should be allowable for at least the same reasons as claim 19. Original claims 14-17 still refer to original claim 10 and should be allowable as indicated by the Examiner.

Applicants respectfully request allowance of claims 1-7 and 10-20.

Please apply any charges or credits to deposit account 06-1050.

Respectfully submitted,

Date: 10/29/03

Arthur Ortega
Arthur Ortega
Reg. No. 53,422

Fish & Richardson P.C.
45 Rockefeller Plaza, Suite 2800
New York, New York 10111
Telephone: (212) 765-5070
Facsimile: (212) 258-2291